XRT84L38ES

The XRT84L38/XRT83L38 8-Channel T1/E1 Framer/LIU Evaluation Board User's Manual

August 23, 2002

THE XRT84L38/XRT83L38 EVALUATION BOARD USER'S MANUAL

XRT84L38ES

The XRT84L38/XRT83L38 8-Channel T1/E1 Framer/LIU Evaluation Board User's Manual

August 23, 2002

1 Introduction

The purpose of this document is to describe the hardware design of the XRT84L38/XRT83L38 8-Channel T1/E1 Framer/LIU Evaluation Board System. This document will briefly discuss features of each of the functioning blocks on the evaluation board system. This document will also describe how to verify proper operation of the XRT84L38 8-Channel T1/E1 Framer IC and the XRT83L38 8-Channel T1/E1 Long-Haul / Short-Haul LIU IC by using the evaluation board system alone or with other testing equipments.

2 Basic Structure of the XRT84L38 8-Channel T1/E1 Framer Evaluation Board

The XRT84L38 8-Channel T1/E1 Framer Evaluation Board is a "PCI Plug-in" board that can be plugged into any standard "PCI" slot within a PC.

The XRT84L38 8-Channel T1/E1 Framer Evaluation Board should consists of the following functioning blocks.

- PCI9030 PCI Bridge (U10) to interface PCI system bus with the evaluation board.
- XC95144XL 144-pin CPLD (U3) to provide glue-logic for the microprocessor interface of framer and LIU.
- Four Spartan XCS20XL 144-pin PQFP FPGAs (U5 – U8) to provide source of data pattern to the framer.
- Eight transformers and RJ45 connectors to interface the LIU with test equipments.
- XRT84L38 8-Channel T1/E1 Framer IC (U4) as the device under test.
- XRT83L38 8-Channel T1/E1 LIU IC (U12) as the device under test.

A simplified drawing of the XRT84L38 8-Channel T1/E1 Framer Evaluation Board is shown below in Figure 1.

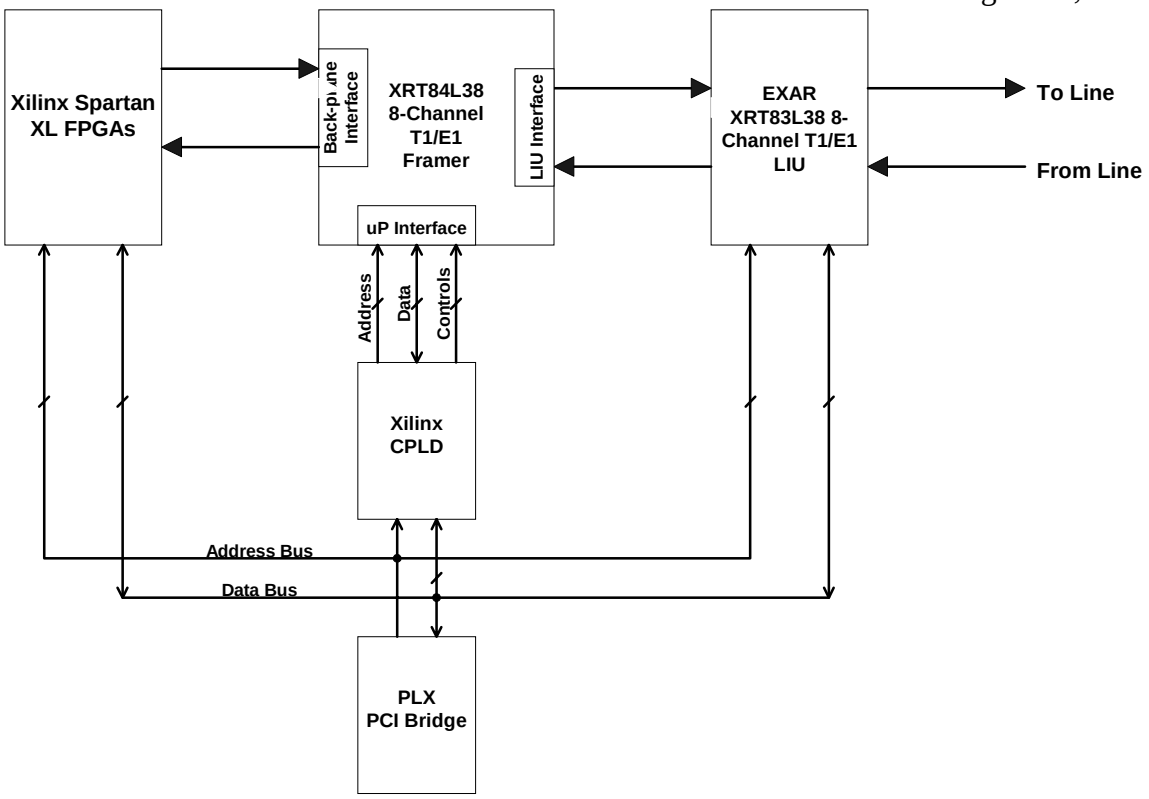


Figure 1. Functional Block Diagram of the XRT84L38 8-Channel T1/E1 Framer Evaluation Board

A brief discussion of each of the functioning blocks of the Evaluation Board System is given below.

2.1 PCI9030 PCI Bridge

The PCI Bridge acts as an interface between the PCI bus master (from the PC) and the local system bus of the Evaluation Board system. It provides necessary bus operation signals such as READ, WRITE, ALE, READY and Chip Select to the functioning blocks on the evaluation block. It also shares the data bus and address bus with all "address-able" components on the evaluation board.

2.2 XC95144XL CPLD

The CPLD performs the following functions:

1. Accepts the bus control signals from the PCI9030 PCI Bridge device and generates microprocessor interface signals to the XRT84L38 Framer device, the XRT83L38 LIU device and each of the four (4) XCS20XL FPGA devices. The CPLD device can be configured to emulate a wide variety of Microprocessors by accepting and generating various control signals with the appropriate timing.

2. Generates the local bus interrupt and READY signals back out to the PCI Bridge device.

3. Generate the chip select signals for each of the four XCS20XL FPGAs on the Evaluation Board.

4. The CPLD device also distributes many of the clock signals that are required by the Evaluation Board circuitry. Such clock signals include the local processor clock (33MHz), the T1 source clock (65.536MHz) and the E1 source clock (49.408MHz).

5. Generates other control signals, such as RESET, TEST MODE for the Framer and LIU devices.

2.3 Spartan XCS20XL FPGA

There are four (4) instantiations of the Spartan XCS20XL FPGA on this Evaluation Board design.

These four FPGAs perform the following functions:

1. In the "Stand-alone" Mode (e.g., when the Evaluation Board has the responsibility of "sourcing" and "terminating" all T1/E1 data) a given FPGA will supply a continuous stream of T1/E1 data its corresponding channel(s) within the Framer device via the TxSer_n serial data input pin. The contents of this T1/E1 data can be a PRBS or a "user-configurable" pattern. Depending on the setting of framer, the FPGA will also generate the TxSync_n, TxSerclk_n and TxMsync_n signals, to the Framer device as well. Additionally, this FPGA will also accept the "received serial" data from the Framer device (which is output via the "RxSer_n" pin). As the FPGA receives this data it will be routed to a "Pattern Receiver" where it will be checked for data integrity. The FPGA will detect and flag the

occurrence of bit-errors by generating an interrupt to the XC95144XL CPDL device.

2. In the "External Tester" Mode (e.g., when the "external" Test Equipment is now configured to be the "source" and "sink" of T1/E1 data), the FPGA will support a "board-loop-back" path by acting as a serial shift register. In this case, serial data (that is received from the RxSer_n output pin of the Framer device) will be routed back to the TxSer_n input pin of Framer and will be in-line with TxSync_n signal. This time, the external tester will be responsible in checking the integrity of data.

3. The FPGA also sources "transmit-direction" signaling bits and processes "receive direction" signaling bits; fractional T1 data, overhead bits generations, as well as CRC generation and checking, framing bits generation and checking.

4. Finally, the FPGA can be configured to function as the as the System Back-plane Master device to which the Framer device is to be interfaced with. The FPGA can exchange data with the Framer device at the following data rates: 1.544Mbits/s, 2.048Mbits/s, 4.096Mbits/s, 8.192Mbits/s, multiplexed 12.352Mbits/s or multiplexed 16.384Mbits/s serial stream. The FPGA also supports the HMVIP/H.100 mode, which is a byte-multiplexed serial stream of 16.384Mbits/s.

2.4 RJ45 Connector and Transformer

The RJ45 Connector and Transformer provide data paths for external Test Equipment to be connected to the Evaluation Board System. By connecting the Receive end and Transmit end of the RJ45 Connector together with twisted-pair cable, the Evaluation Board System can perform loop-back operations.

2.5 XRT84L38 T1/E1 8-Channel Framer Device

On the transmit side, the XRT84L38 T1/E1 8-Channel Framer accepts raw payload data from the Terminal Equipment (or from the FPGAs on the Evaluation Board). The framer then inserts Framing bits, CRC bits, LAPD or BOS messages and robbed signaling bits into the data stream. Finally, the DS1 or E1 data are AMI or B8Z3 or HDB3 encoded and sent to the LIU either bipolar or single-railed.

On the receive side, bipolar or single-railed data are taken into the framer device from the LIU. The Framer device extracts the framing bits, CRC bits, LAPD or BOS messages and robbed signaling bits from the incoming data stream. Payload data and/or the Framing bits, Data Link messages and signaling bits are sent to the Terminal Equipment (or the FPGAs on the Evaluation Board).

2.6 XRT83L38 T1/E1 8-Channel Long-Haul/Short-Haul LIU

The LIU transmits and receives T1/E1 line signals through the transformers and RJ45 connector to external test equipment. For "Cable-Loop-back" operation, two channels can be connected together by wiring the Transmit section of one channel to the Receive section of another channel.

3 Basic Operation of the Evaluation Board System

EXAR has developed Graphical User Interface (GUI) software to control operation of the XRT84L38/XRT83L38 Evaluation Board System. The user can configure the XRT84L38 framer device and the XRT83L38 LIU device to run various kinds of test and thus verify their functionalities. Some of the tests supported by the GUI software are listed below:

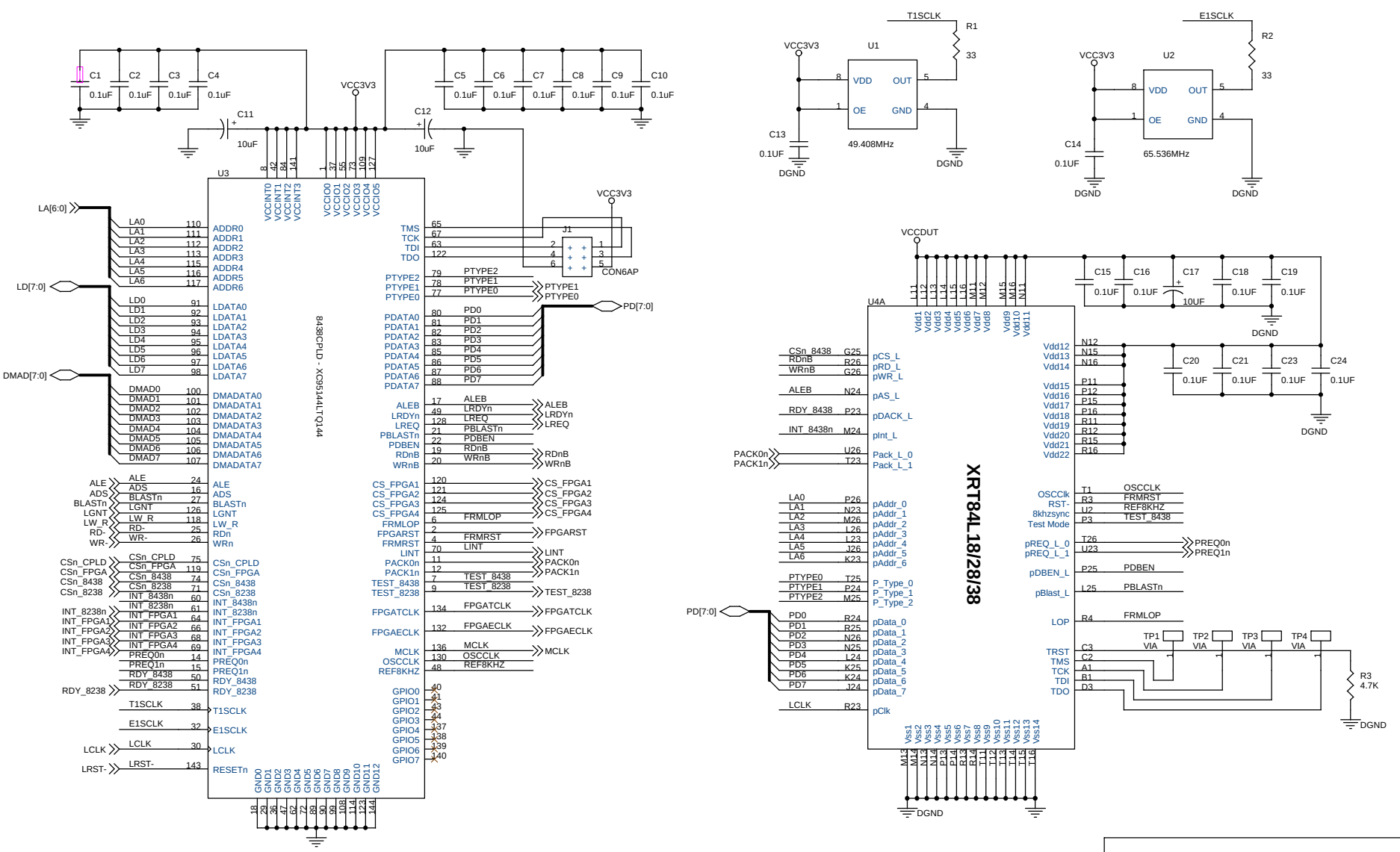
- Framing Format Configuration
- Signaling Bit Insertion and Extraction in T1 mode
- Transmitting and Receiving of Bit-Oriented Signaling (BOS) Messages
- Transmitting and Receiving of LAPD Messages
- Transmitting and Receiving of CAS in E1 mode
- Various Alarm Generation and Detection
- Performance Monitoring

Details of how to configure the Evaluation Board System using the GUI software will be discussed in the XRT84L38 Software User Manual.

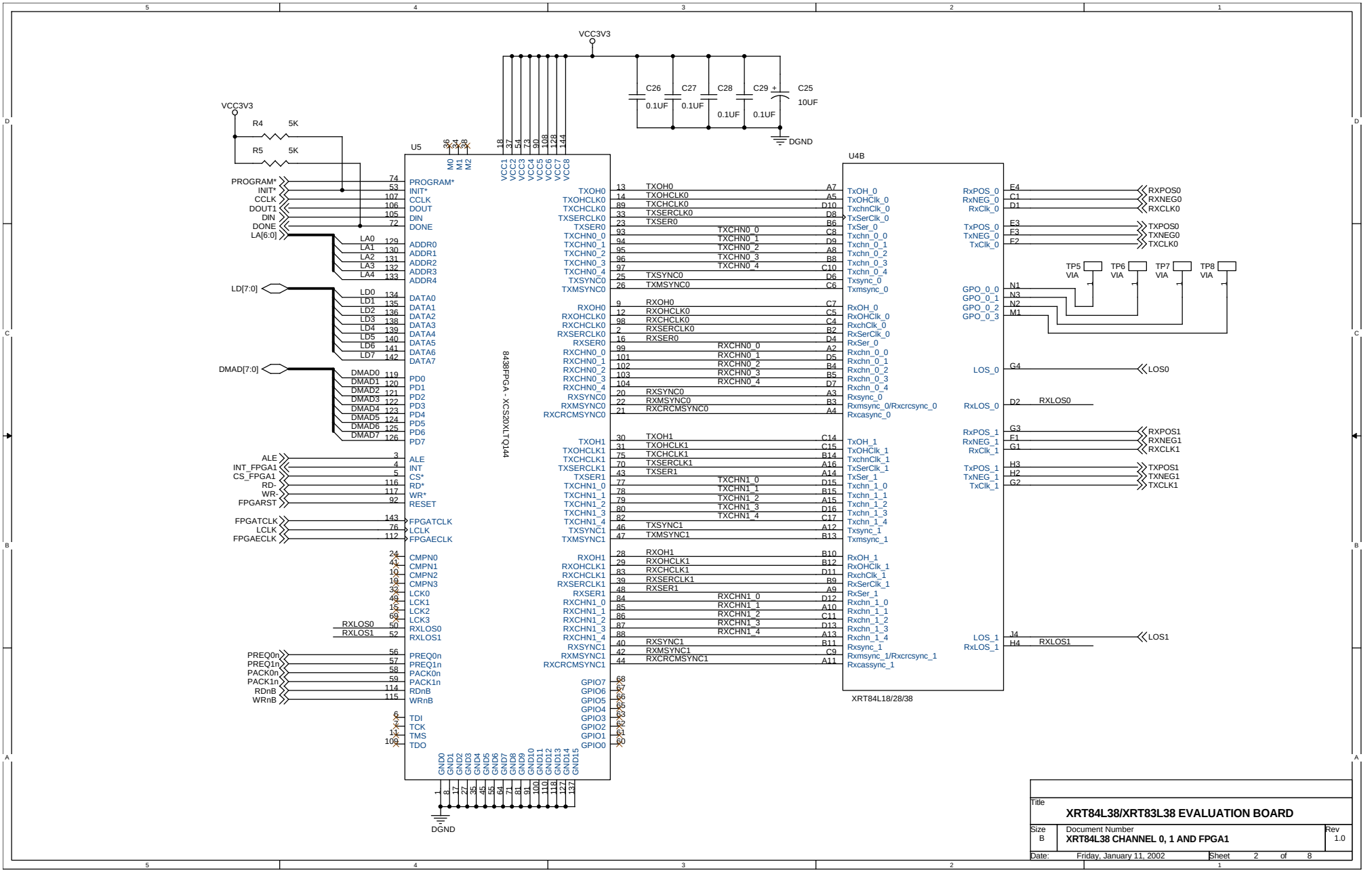
The XRT84L38/XRT83L38 8-Channel T1/E1 Framer/LIU Evaluation Board User's Manual

August 23, 2002

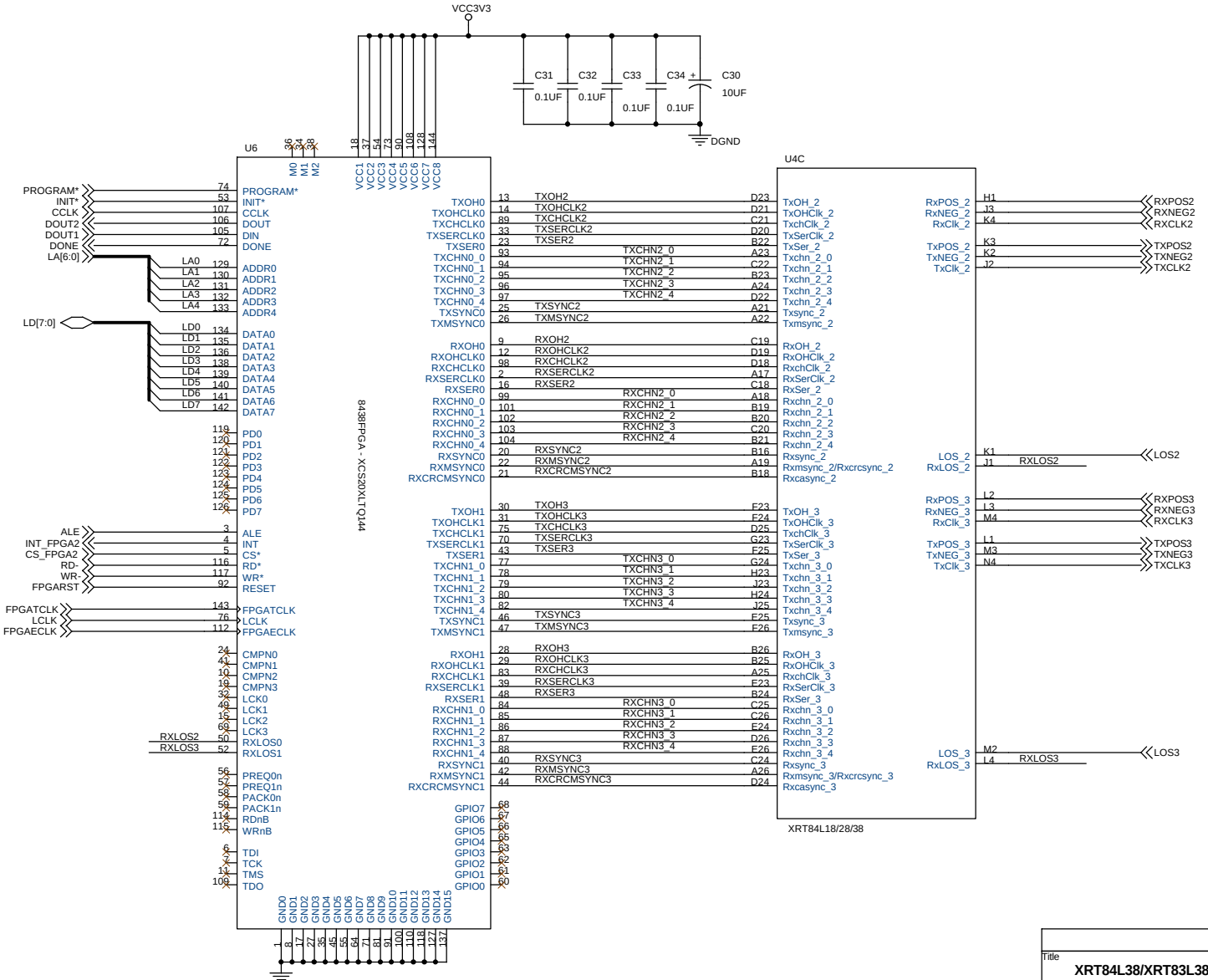
THE SCHEMATIC DESIGN OF THE XRT84L38 EVALUATION BOARD



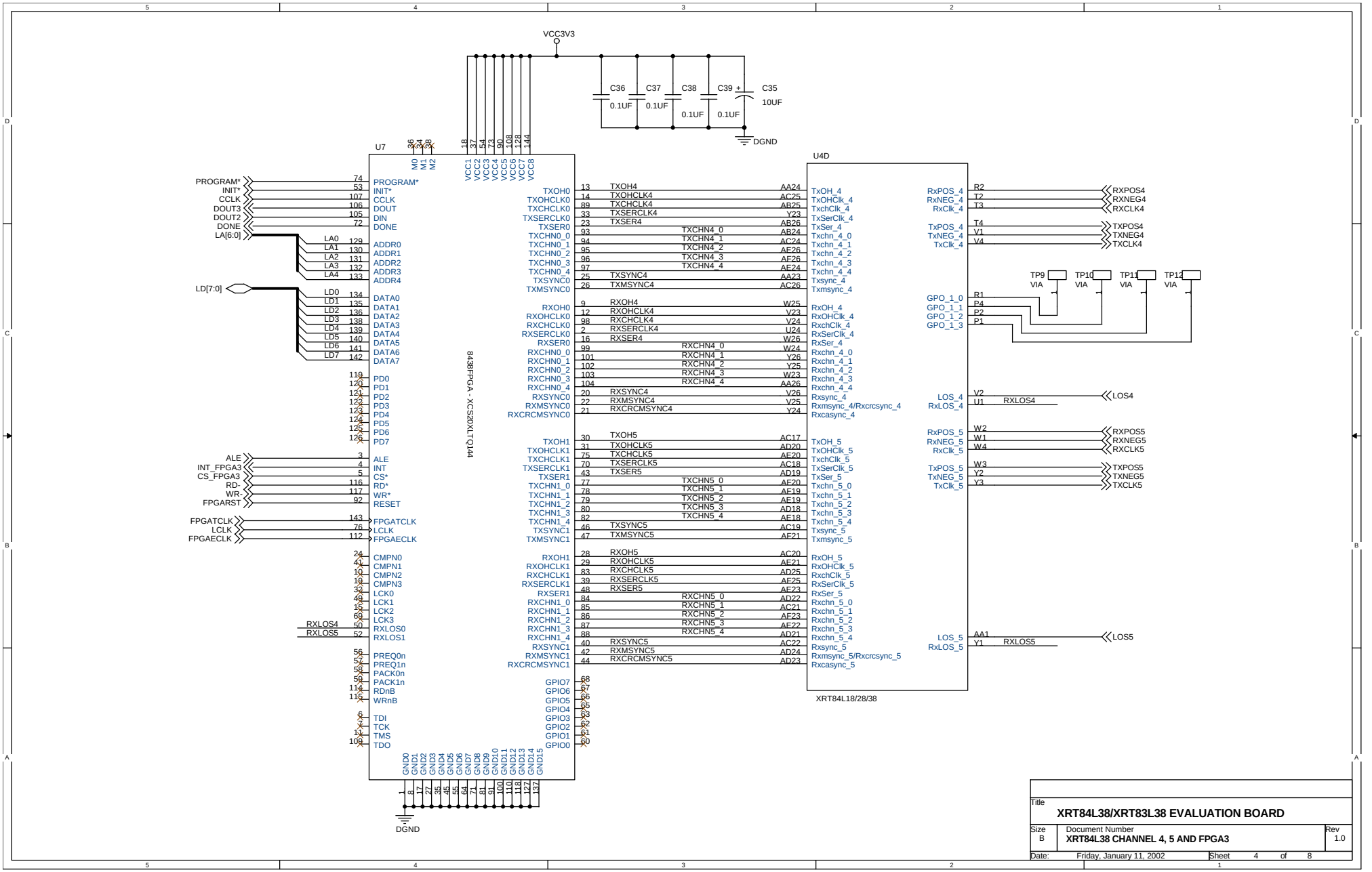
Title	XRT84L38/XRT83L38 EVALUATION BOARD
Size B	Document Number CPLD / FRAMER MICROPROCESSOR INTERFACE
Rev	1.0
Date:	Friday, January 11, 2002
Sheet	1 of 8



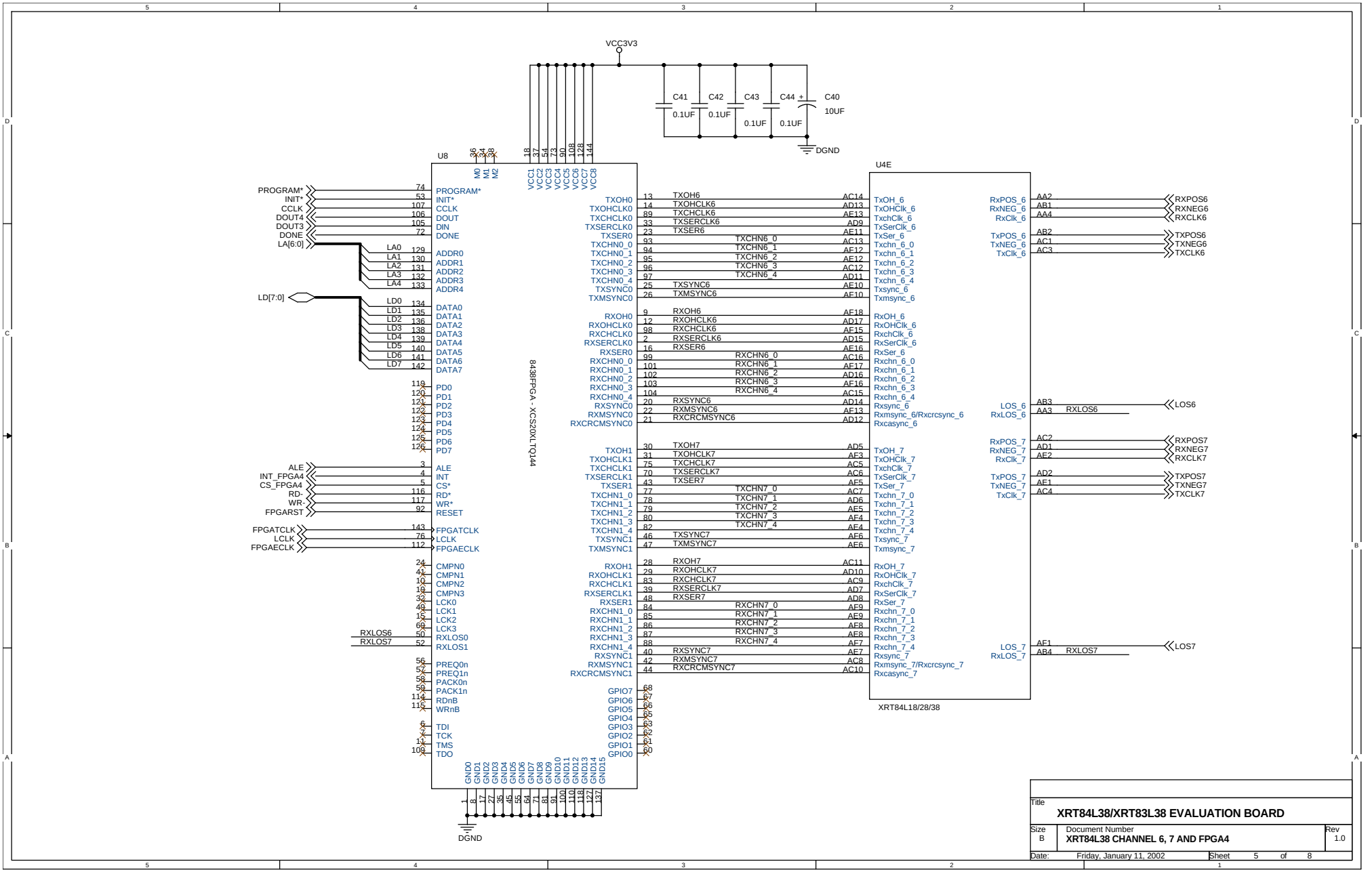
Title	XRT84L38/XRT83L38 EVALUATION BOARD	
Size B	Document Number XRT84L38 CHANNEL 0, 1 AND FPGA1	Rev 1.0
Date: Friday, January 11, 2002	Sheet 2 of 8	



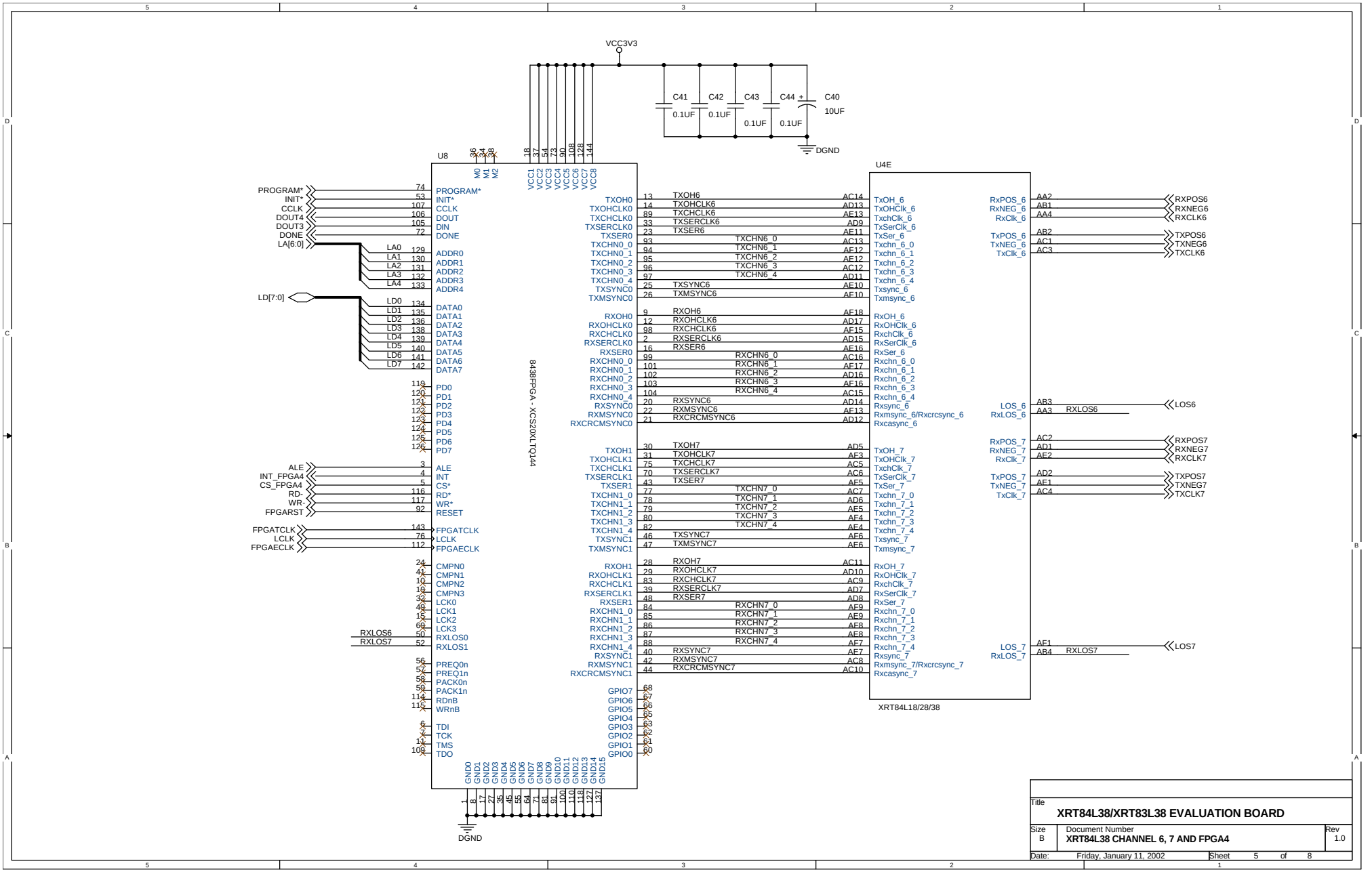
Title	**XRT84L38/XRT83L38 EVALUATION BOARD**
Size B	Document Number **XRT84L38 CHANNEL 2, 3 AND FPGA2** Rev 1.0
Date: Friday, January 11, 2002	Sheet 3 of 8



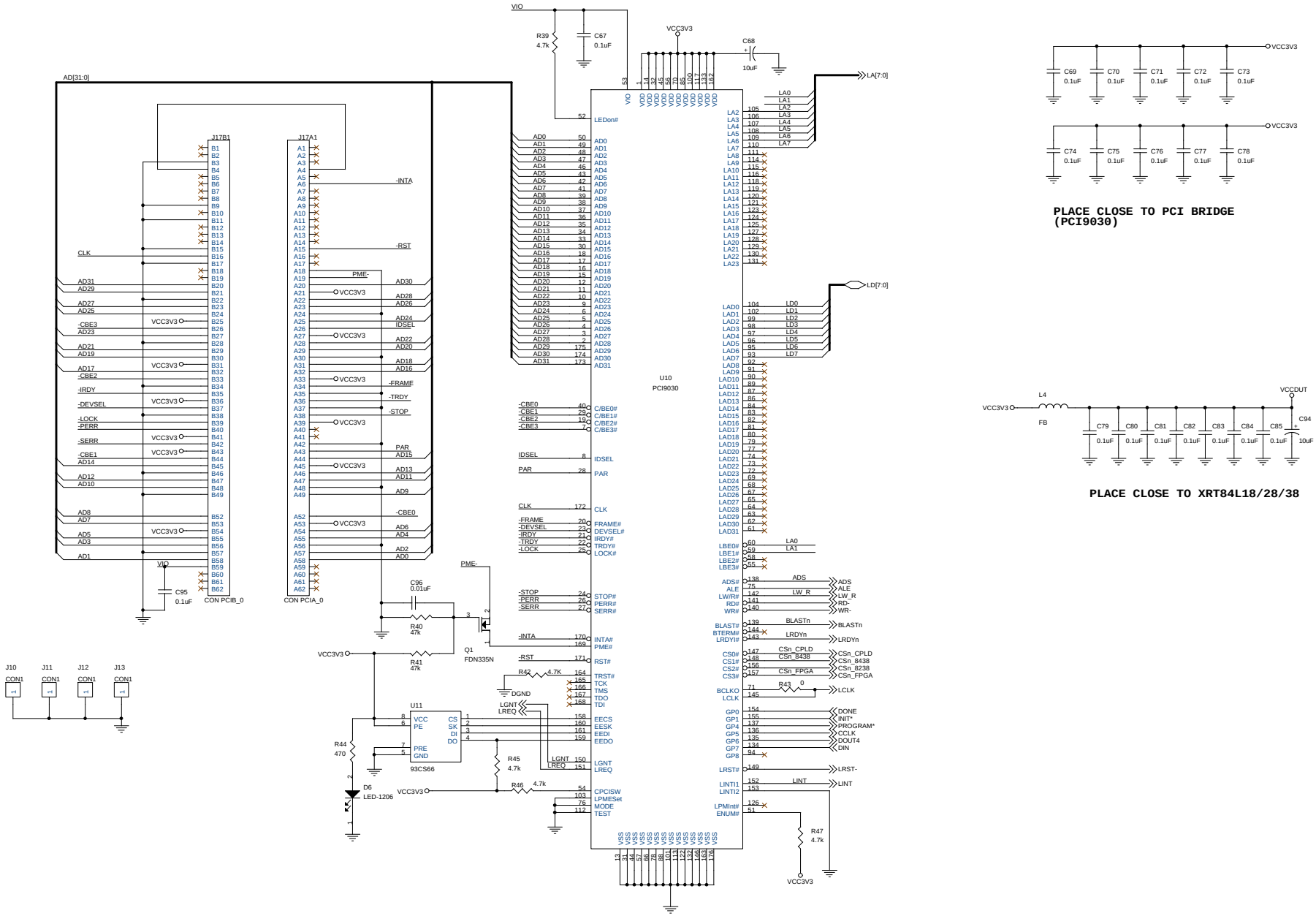
Title	**XRT84L38/XRT83L38 EVALUATION BOARD**
Size B	Document Number **XRT84L38 CHANNEL 4, 5 AND FPGA3** Rev 1.0
Date: Friday, January 11, 2002	Sheet 4 of 8



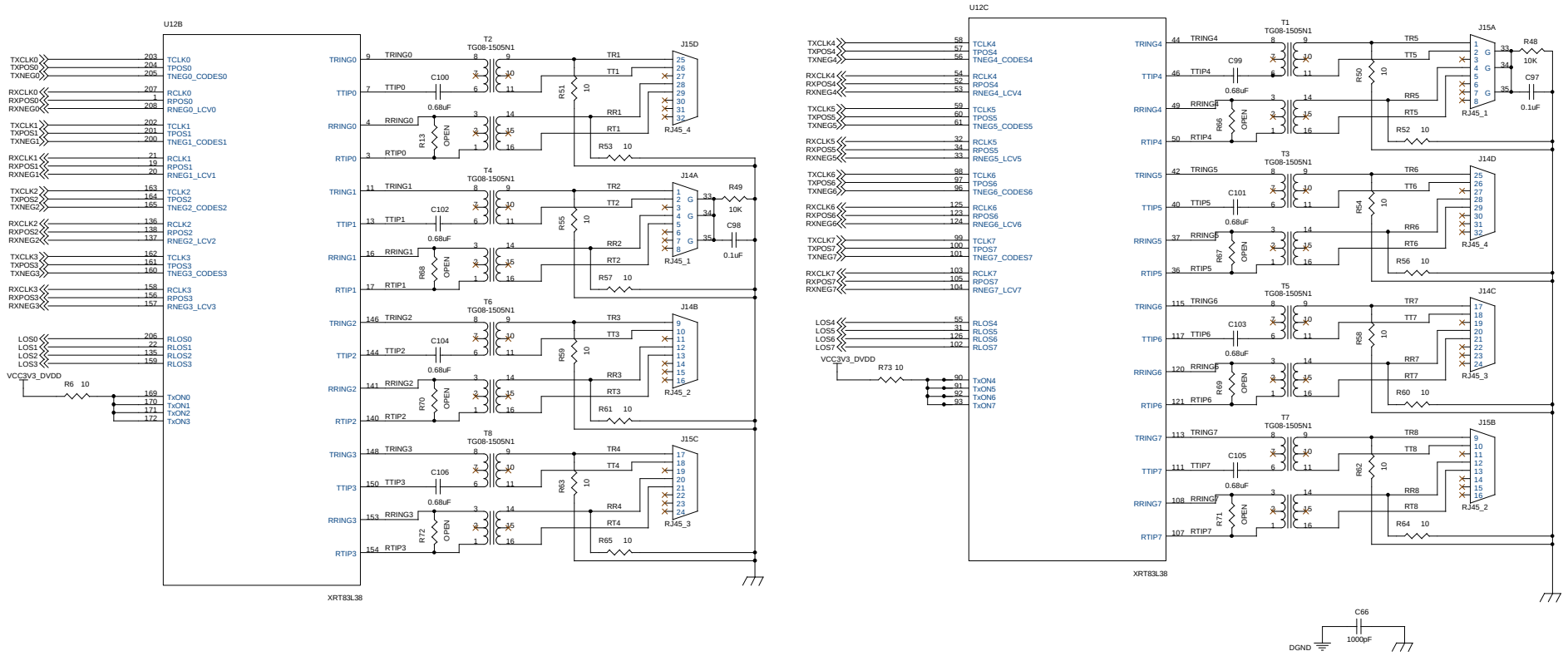
Title	**XRT84L38/XRT83L38 EVALUATION BOARD**
Size B	Document Number **XRT84L38 CHANNEL 6, 7 AND FPGA4** Rev 1.0
Date: Friday, January 11, 2002	Sheet 5 of 8



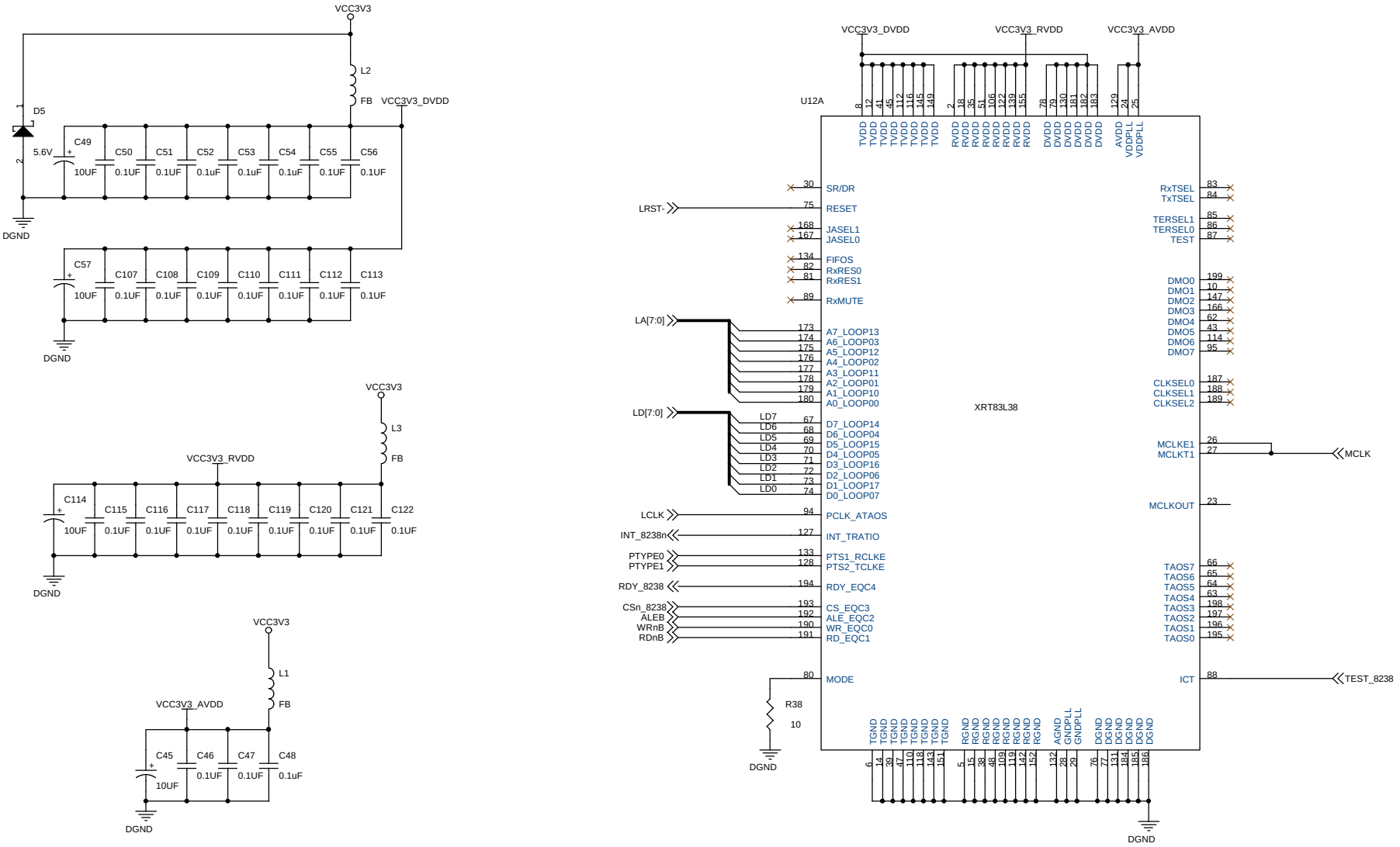
Title	**XRT84L38/XRT83L38 EVALUATION BOARD**
Size B	Document Number **XRT84L38 CHANNEL 6, 7 AND FPGA4** Rev 1.0
Date: Friday, January 11, 2002	Sheet 5 of 8



Title	XRT84L38/XRT83L38 EVALUATION BOARD	
Size C	Document Number PCI INTERFACE	Rev 1.0
Date: Friday, January 11, 2002	Sheet 8 of 8	



Title	XRT84L38/XRT83L38 EVALUATION BOARD	
Size: C	Document Number: XRT83L38 8 CHANNEL LINE INTERFACE UNIT	Rev: 1.0
Date: Friday, January 11, 2002	Sheet 6 of 8	



Title	**XRT84L38/XRT83L38 EVALUATION BOARD**
Size B	Document Number **XRT83L38 8 CHANNEL LINE INTERFACE UNIT**
Rev	1.0
Date:	Friday, January 11, 2002
Sheet	7 of 8